SPLIT GATE SOURCE SIDE INJECTION

ABSTRACT OF THE DISCLOSURE

Novel memory cells utilize source-side injection, allowing very small programming currents. If desired, to-be-programmed cells are programmed simultaneously while not requiring an unacceptably large programming current for any given programming operation. In one embodiment, memory arrays are organized in sectors with each sector being formed of a single column or a group of columns having their control gates connected in common. In one embodiment, a high speed shift register is used in place of a row decoder to serially shift in data for the word lines, with all data for each word line of a sector being contained in the shift register on completion of its serial loading. In one embodiment, speed is improved by utilizing a parallel loaded buffer register which receives parallel data from the high speed shift register and holds that data during the write operation, allowing the shift register to receive serial loaded data during the write operation for use in a subsequent write operation. In one embodiment, a verification is performed in parallel on all to-be-programmed cells in a column and the bit line current monitored. If all of the to-be-programmed cells have been properly programmed, the bit line current will be substantially zero. If bit line current is detected, another write operation is performed on all cells of the sector, and another verify operation is performed. This write/verify procedure is repeated until verification is successful, as detected or substantially zero, bit line current.